In the Claims:

Please rewrite the claims as follows:

1-5. (Canceled)

6. (Original) An error checking system comprising:

an input device for receiving a data element including parity information;

a parity check device for checking the parity information of the data element to determine whether the data element is valid;

a CRC generator coupled to the parity check device for generating a CRC for the data element; and

an output device for transmitting the data element with the parity information and CRC to a downstream device over a transmission link;

wherein the parity check device is operative to output a corruption signal to the CRC generator if the parity check device determines that the data element is invalid, to instruct the CRC generator to corrupt the CRC generation for that data element.

7. (Original) The error checking system of claim 6 further comprising an alarm device for transmitting an alarm signal to the downstream device when the CRC for a particular data element has been corrupted.

8. (Original) The error checking system of claim 6 wherein the CRC generator corrupts a CRC by flipping a bit of an associated original CRC generated for a particular data element.

9. (Original) The error checking system of claim 7 wherein the downstream device, upon receiving the alarm signal, resynchronizes the transmission link.

10-13. (Canceled)

14. (Original) A data transmission system comprising:

a data transmission device for transmitting data elements to a downstream device;

a data reception device for receiving data elements from the downstream device, the data reception device including:

an input CRC checking device coupled to receive the data elements from the downstream device for checking the validity of received data elements based on a CRC associated with each received data element;

a memory device coupled to the input CRC checking device for storing data elements received from the downstream device after the data elements have been processed by the input CRC checking device; and

an output CRC checking device coupled to receive the data elements from the memory device for checking the validity of the data elements based on the CRC associated with each data element.

15. (Original) The system of claim 14 wherein, if an invalid data element is detected by the input CRC checking device, the input CRC checking device notifies the data transmission device that at least one data element received by the data reception device is invalid.

16. (Original) The system of claim 15 wherein the memory device includes a First In-First Out (FIFO) memory device.

17. (Original) The system of claim 16 wherein the data reception device includes a first data element processing path and a second data element processing path for processing different portions of the received data elements.

18. (Original) The system of claim 17 wherein the input CRC checking device includes a first CRC checking unit coupled to the first data element processing path and a second CRC checking unit coupled to the second data element processing path.

19. (Original) The system of claim 18 wherein the FIFO memory device includes a first FIFO memory unit coupled to the first data element processing path for receiving data elements from the first CRC checking unit and a second FIFO memory unit coupled to the second data element processing path for receiving data elements from the second CRC checking unit.

20. (Original) The system of claim 19 wherein the first data element processing path processes the high bits of the received data elements and the second data element processing path processes the low bits of the received data elements.